Experiment 1: pn Junction Capacitance

Safety
The voltages used in this experiment are less than 15 V and normally do not present a risk of shock. However, you should always follow safe procedures when working on any electronic circuit. Assemble or modify a circuit with the power off or disconnected. Don’t touch different nodes of a live circuit simultaneously, and don’t touch the circuit if any part of you is grounded. Don’t touch a circuit if you have a cut or sore that might come in contact with a live wire. Check the orientation of polarized capacitors before powering a circuit, and remember that capacitors can store charge after the power is turned off. Never remove a wire from an inductor while current is flowing through it. Components can become hot if a fault develops or even during normal operation so use appropriate caution when touching components.

Objectives: This laboratory exercise will investigate the capacitance of a pn junction. At the end of the laboratory a student should be able to relate measurements of the capacitance to the theory governing the junction and the internal structure of the junction. The student should also become familiar with a varactor, which is a useful device for tuning circuits.

Introduction: After bringing a p-type semiconductor together with an n-type semiconductor to form a pn junction, diffusion currents cause holes from the p-side to flow to the n-side and electrons from the n-side to flow to the p-side. These infused minority carriers recombine with the majority carriers leading to a region on both sides of the junction that is depleted of carriers called appropriately enough the depletion region. The diffusion currents also cause a separation of charge with the p-side of the depletion region becoming negatively charged and the n-side becoming positively charged. The electric field created causes a drift current that opposes the diffusion current. When the two currents are in balance, a new equilibrium is reached. An unbiased pn junction is depicted in Fig. 6.1 in the textbook.

The width of the depletion region is determined by the doping levels \( N_a \) and \( N_d \) in the semiconductor.

\[
w = \left( \frac{2\varepsilon (N_a + N_d)V_0}{eN_aN_d} \right)^{1/2}
\]

where \( V_0 \) is the electric potential difference across the junction, the so-called built-in potential, and \( \varepsilon = \varepsilon_R \varepsilon_0 \) the dielectric constant of the semiconductor times the permittivity of free space.

\[
V_0 = \left( \frac{kT}{e} \right) \ln \left( \frac{N_aN_d}{n_i^2} \right)
\]

Applying an external bias voltage adds or subtracts from the built-in potential leading to a new equilibrium. A reverse bias increases \( V_0 \) leading to an increase in the depletion width whereas a forward bias decreases \( V_0 \) and the depletion width.
Because the depletion region is charged positively on one side and negatively on the other, it resembles a parallel-plate capacitor, except that the charge is distributed over a volume rather than being on plates, and thus we expect a capacitance to be associated with the junction. What makes this capacitance interesting is that it can be changed by applying a bias voltage leading to a voltage-tunable capacitor. Such a device is called a varactor and it finds applications in voltage-controlled oscillators and tuned rf circuits.

The charge stored on each side is fairly easy to work out from the doping levels.

\[ |Q| = eN_d w_n A = eN_a w_p A \]

where \( w_n \) and \( w_p \) are the depletion widths on the n-side and the p-side respectively. Since the total depletion width equals the sum of the individual widths, \( Q \) can be related to the applied voltage through the equation for the depletion width.

\[ w = w_n + w_p = \frac{Q}{eA} \left( \frac{1}{N_d} + \frac{1}{N_a} \right) = \left[ \frac{2e(N_a + N_d)(V_0 - V)}{eN_aN_d} \right]^{1/2} \]

where now the applied voltage \( V \) is included. From this equation, the capacitance \( Q/V \) can be calculated; notice that the capacitance is a function of voltage.

In many applications and in this lab, the total junction capacitance is not of interest but rather the small-signal or differential capacitance. The differential capacitance involves a small change in voltage causing a small change in charge stored \( dQ \); \( C = dQ / dV \). Differentiating the above equation gives this capacitance.

\[ C = \frac{dQ}{dV} = \frac{A}{(V_0 - V)^{1/2}} \left( \frac{e\epsilon N_aN_d}{2(N_a + N_d)} \right)^{1/2} \]

Procedure:

We want to verify the above equation for various diodes including some varactors. All pn junction diodes have junction capacitance. Certain diodes are designed to have a large capacitance that varies significantly with applied reverse bias. These are called varactors and are used in circuits that need a voltage controlled capacitance.

To measure the capacitance, set up the following circuit.

The circuit measures capacitance by measuring the resonance frequency of a tank circuit consisting of the diode’s capacitance the 100pF capacitor and the inductor,
\[ \omega_r = (LC)^{1/2} \text{ where } C = C_{\text{diode}} + 100\text{pF} \]

(Why is the 100nF capacitor not included?) The d.c. voltage is applied to the diode via the terminal connected to AWG1. The 56K resistor prevents the d.c. supply from shorting the tank circuit; it needs to be large compared to the tank circuit's impedance at resonance. The 100nF capacitors block d.c. from the inductor and the op-amp; they need to be large compared to the diode's capacitance. The tank circuit is excited by a small a.c. signal via AWG2. The op-amp amplifies the tank circuit voltage by 10.

For each diode, you should look at the manufacturer's data sheet for the nominal capacitance (not always given) and estimate the resonance frequency. Excite the tank circuit with a small-signal sine wave. The signal must be less than the thermal voltage, 25 mV. Vary the frequency and look for the peak in the resonance. From the frequency, calculate the capacitance. Repeat the measurement for different d.c. voltages \( V_{dc} \). Investigate both reverse bias and forward bias (forward bias is limited by the current that can be supplied to the diode through the 56K resistor). Compare your results with the equation above by graphing \( 1/C^2 \) vs. \( V_{dc} \). What is the built-in potential? Use the data sheet or reasonable assumptions to estimate the doping levels in the device.